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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,250	08/17/2001	Fumikazu Takahashi	500.40501X00	2734

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EXAMINER	
COX, CASSANDRA F	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,250	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is indefinite because the phrase "a node arranged in the vicinity of an input terminal of the gate circuit connected to an input terminal of the driver circuit" is misdescriptive. A node in the vicinity of an input terminal of the gate circuits would be connected to the output of the driver circuit rather than the input. Furthermore, it appears to the examiner that the "second long-distance wiring" receives the input signal at the input node of the driver circuit. Correction or clarification is required.

Claims 2-9 are also rejected due to the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United

States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi et al (U.S. Patent No. 6,088,286).

In reference to claim 1, Yamauchi discloses in Figure 20 a semiconductor integrated circuit device comprising a driver circuit (10a), a first long-distance wiring (MWL) connected to the driver circuit, and a plurality of gate circuits (MC, shown in Figure 5) connected over the entire length of the first long-distance wiring, so that an input signal (VB) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring, wherein the input node and an end of the first long-distance wiring is connected by a second long-distance wiring (SWL) and a speed-increasing circuit (11za).

In reference to claim 8, Yamauchi discloses in column 6, lines 17-21 that the input signal is a word line selecting signal; the driver is realized by a word line driver (10a, figure 20); the first long-distance wiring is realized by a word line (MWL); and the gate circuits are realized by memory cells (MC, figure 5).

5. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Huber (U.S. Patent No. 6,366,520).

In reference to claim 1, Huber discloses in Figure 7 a circuit comprising a driver circuit (110), a first long distance wiring (which is seen as the wire carrying the output of driver 110), and a plurality of gate circuits (180, 188, 182 and 128) connected over the entire length of the first long-distance wiring, so that an input signal is received by the plurality of gate circuits via the driver circuit (110) and the first long-distance wiring,

wherein the input node and an end of the first long-distance wiring is connected by a second long-distance wiring (which is seen as the wire carrying the input signal to the buffer 160 and transistors 166 and 161) and a speed-increasing circuit (166).

In reference to claim 2 Huber discloses in Figure 7 that the speed-increasing circuit (166) is a PMOS transistor.

Allowable Subject Matter

6. Claims 3-7 and 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claim 3 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the speed increasing circuit includes an NMOS transistor (110) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 4 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 10 wherein the speed increasing circuit includes a CMOS inverter (113) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 5 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 that includes a plurality of speed increasing

circuits (107) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 6 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein a plurality of buffer circuits (200, 201) are inserted at the input side of the second long-distance wiring (106) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 7 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 6 wherein a buffer circuit (201) is inserted at the output side of the second long-distance wiring (106) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 9 wherein the gate circuits (203) are realized by flip-flop circuits in combination with the rest of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-

872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

April 7, 2002

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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